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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KANG, DONGHEE	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/473,394	MISTRY, KAIZAD R.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- Th MAILING DATE of this communication app ars on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 26, 2004 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims7-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The phrase "a gate dielectric layer ...and superjacent a portion of a top surface of the substrate" is not supported by the disclosure. The gate dielectric layer 411 is disposed superjacent the curvilinear but not the top surface of the substrate (see fig.4).

Claims 8-9 are rejected because each includes the limitations of independent claim 7.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 4-6 are rejected under 35 U.S.C. 102(a) as being anticipated by Gardner et al. (US 5,918,134).

Regarding claim **4**, Gardner et al. disclose a field effect transistor, comprising (Fig.10):

a substrate (102) having a recess in a surface thereof; the recess having a bottom portion and tapered sidewalls, the tapered sidewall surface forming an obtuse angle with respect to the bottom portions of the recess; a gate dielectric layer (132) disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls, and superjacent a portion of a top surface of the substrate; a gate electrode (134) completely overlying the gate dielectric layer; and source/drain terminals (140a) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls; wherein the source/drain terminals comprises an extension (130) which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to sidewalls of the recess, a portion of the gate dielectric layer overlying an innermost portion of the extension.

The word "adjacent" is a broad term, which means not distant or nearby (Merriam-Webster's Collegiate Dictionary). Figure 10 clearly shows that the entire innermost side of the extension is adjacent to the tapered sidewalls of the recess.

Regarding claim **5**, Gardner et al. disclose that a portion of the gate electrode overlies an innermost portion of extension.

Regarding claim **6**, Gardner et al. discloses that the gate electrode conforms to a recessed channel.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 6,303,448) in view of Jeuch et al. (US 4,939,100)

Regarding claim **1**, Chang et al. disclose a field effect transistor, comprising (Fig.6):

a substrate (10) having a recess in a surface thereof; the recess having a bottom portion and substantially vertical sidewalls; a gate dielectric layer (62) disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls; a gate electrode (64A) completely overlying the gate dielectric layer; and source/drain terminals (70) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth

within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprises an extension (LDD,66) which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to the vertical sidewalls of the recess, a portion of the gate dielectric layer overlying an innermost portion of the extension.

The word "adjacent" is a broad term, which means not distant or nearby (Merriam-Webster's Collegiate Dictionary). Figure 6 clearly shows that the entire innermost side of the extension is adjacent to the sidewalls of the recess.

Chang et al. do not teach the gate dielectric layer disposed superjacent a portion of a top surface of the substrate. Jeuch et al. teach in Fig. 5I the gate dielectric layer (56) disposed superjacent the bottom portion of the recess and superjacent a portion of a top surface of the substrate to reduce an electric field (Col.5, lines 53-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Jeuch into the Chang's device in order to reduce the electric field.

Regarding claim **2**, Chang et al. disclose the transistor further comprising a portion of the gate electrode that overlies the innermost portion of the extension.

Regarding claim **3**, Chang et al. disclose that the gate electrode conforms to a recessed channel.

Response to Arguments

8. Applicant's arguments with respect to claims 1-3 & 7-9 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed April 26, 2004 have been fully considered but they are not persuasive. Applicant argues that Gardner does not teach "a gate dielectric layer disposed superjacent the bottom portion of the recess, adjacent the tapered sidewalls, and *superjacent a portion of a top surface of the substrate*". This is not convincing. Gardner et al. clearly teach in Fig.10 the dielectric layer 132 disposed a portion of top surface of the substrate.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D
Primary Examiner
Art Unit 2811

dhk